EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 06150666
PUBLICATION DATE : 31-05-94

APPLICATION DATE : 12-11-92
APPLICATION NUMBER : 04302369

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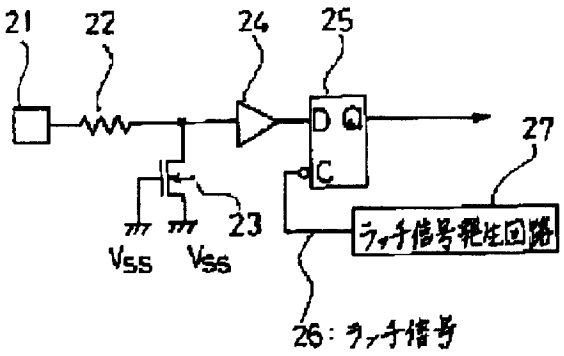
INT.CL. : G11C 11/413 G11C 11/417 H03K 19/0175 H03K 19/003

TITLE : INPUT CIRCUIT



ABSTRACT : PURPOSE: To prevent erroneous operation due to a noise generated from an input buffer circuit in the period in which an output buffer executes switching by decreasing the resistance value of an input resistor connected to an input terminal.

CONSTITUTION: An input resistor 22 connected to an input terminal 21, an input buffer circuit 24 connected to the input resistor 22, a latching circuit 25 connected between the input buffer circuit 24 and an internal circuit and a latching signal generating circuit 27 supplying a latching signal 26 to the latching circuit 25 are provided. By generating the latching signal 26 in the period in which the output buffer circuit switches by means of the latching signal generating circuit 27, the latching circuit 25 interrupts a noise outputted from the input buffer circuit 24, latches and holds the input signal before the generation of the noise. Consequently, the transfer of the noise outputted from the input buffer circuit 24 in the period in which the output buffer circuit switches to the internal circuit is prevented.

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CLAIMS

[Claim(s)]
[Claim 1] It is the input circuit which possesses the latch circuit connected between the input-buffer circuit which is an input circuit for preventing malfunction by the noise generated at the switching period of an output-buffer circuit, and was connected to the input terminal through input resistance, and said input-buffer circuit and internal circuitry, and the latch signal generating circuit for supplying a latch signal to said latch circuit, and is characterized by for said latch signal generating circuit to generate a latch signal at the period which an output-buffer circuit switches.
[Claim 2] It is the input circuit according to claim 1 which is applied to the input circuit of the address terminal of a SRAM semiconductor integrated circuit, and is characterized by for said latch signal delaying the ATD signal which a SRAM semiconductor integrated circuit has, and generating it.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the input circuit which prevented malfunction by the noise generated by switching of an output-buffer circuit in semiconductor integrated circuits, such as SRAM, about a semiconductor integrated circuit.
[0002]
[Description of the Prior Art] Drawing 4 is drawing showing the general input circuit in semiconductor integrated circuits, such as the conventional SRAM (Static Randam Access Memory). (1) is connected to the internal circuitry to which input resistance and (3) are input-buffer circuits, and an input terminal and (2) do not illustrate the output in drawing. (4) is the N-channel MOS transistor, the drain is connected between the end of input resistance (2), and the input of an input-buffer circuit (3), and both the source and the gate are connected to the touch-down electrical potential difference Vss.
[0003] If it was in the input circuit based on the configuration mentioned above, the main role of input resistance (2) and the N-channel MOS transistor (4) prevents destruction of an input-buffer circuit (3) and the internal circuitry which is not illustrated from the excessive abnormal voltage impressed to an input terminal (1), and, as for the resistance, it was conventionally common as input resistance (2) to have formed in about R=1.5kohm-2.0kohm.
[0004] Moreover, the capacity C1 and C2 shown in drawing 4 is parasitic capacitance formed in a node (a). It is what consists of the wiring capacity of a node (a), the drain diffused-junction capacity of the N-channel MOS transistor (4), the gate capacitance of an input-buffer circuit (3), etc. Capacity C1 exists as supply voltage Vdd and a coupling capacity between nodes (a), and capacity C2 exists as the touch-down electrical potential difference Vss and a coupling capacity between nodes (a).
[0005] By the way, if it is in semiconductor integrated circuits, such as SRAM, in recent years, instead of the conventional poly silicon gate, the gate and wiring are formed by the refractory metal silicide of low resistance etc. for the purpose of improvement in working speed. For this reason, the resistance of input resistance (2) is small as compared with the former. This is because pattern area of input resistance (2) cannot be enlarged in order to raise the accumulation consistency of a semiconductor integrated circuit. However, when the resistance of input resistance (2) became small, the problem of becoming easy to malfunction by the power-source noise by switching of the output-buffer circuit which semiconductor integrated circuits, such as SRAM, have occurred.
[0006] Then, the invention-in-this-application person considered the cause as follows. When an output-buffer circuit switches, a big current flows temporarily in a semiconductor integrated circuit, and this power-source noise happens, when a drop or the touch-down electrical potential difference Vss rises [supply voltage Vdd] by this. For this reason, threshold voltage Vt* of an input-buffer circuit (3) Potential is changed. Since the force of holding the potential of the input signal impressed to the input terminal (1) by the node (a) was comparatively weak when the resistance of input resistance (2) was conventionally formed in R=1.5kohm-2.0kohm and a big value, the potential of threshold voltage Vt* of an input-buffer circuit (3) descends by the drop of supply voltage Vdd, and the potential of a node (a)

also descends according to the coupling effectiveness of parasitic capacitance C1.
[0007] On the other hand, the potential of threshold voltage Vt* of an input-buffer circuit (3) rises by lifting of the touch-down electrical potential difference Vss, and the potential of a node (a) also rises according to the coupling effectiveness of parasitic capacitance C2. Therefore, since the potential of the input signal in a node (a) is interlocked with fluctuation of the potential of threshold voltage Vt* of an input-buffer circuit (3) and is changed in the same direction, relation with normal potential of an input signal and potential of threshold voltage Vt* of an input-buffer circuit (3) in a node (a) is maintained. This had become a comparatively strong thing to the power-source noise by switching of an output-buffer circuit.
[0008] However, if the resistance of input resistance (2) becomes small, the force of holding the potential of the input signal impressed to the input terminal (1) by the node (a) will become strong. The drop of the potential of threshold voltage Vt* of the input-buffer circuit (3) by the drop of supply voltage Vdd, Or it is maintained at potential almost equal to the potential of the input signal which lifting of the potential of threshold voltage Vt* of the input-buffer circuit (3) by lifting of the touch-down electrical potential difference Vss was interlocked with, and the potential of a node (a) stopped being able to change easily in the same direction, and was impressed to the input terminal (1). It becomes impossible for this reason, to maintain the normal relation of the potential of the input signal in a node (a), and the potential of threshold voltage Vt* of an input-buffer circuit (3). For this reason, a noise will be outputted from an input-buffer circuit (3). Drawing 5 is a wave form chart showing generating of this noise of operation. As for (11), in drawing, (12) is the output of an output-buffer circuit about the output of an input-buffer circuit (3) in the input signal with which (10) is impressed to an input terminal (1). For the reason mentioned above when it switched, as the output signal of an output-buffer circuit showed by (13) of drawing 5 now, as shown in (14), a noise will be outputted from an input-buffer circuit (3), and it will be transmitted to an internal circuitry, and becomes the cause of malfunction.
[0009]
[Problem(s) to be Solved by the Invention] Thus, if it was in the conventional input circuit, when the resistance of the input resistance (2) which constitutes an input circuit by using the refractory metal silicide of low resistance etc. instead of the conventional polish recon for the purpose of improvement in working speed became small, it had the trouble of becoming easy to produce malfunction, by transmitting the noise outputted by switching of an output-buffer circuit from an input-buffer circuit (3) to an internal circuitry.
[0010]
[Means for Solving the Problem] The input resistance which it succeeded in this invention in view of the above-mentioned trouble, and was connected to the input terminal (21) (22), The latch circuit connected between the input-buffer circuit (24) connected to said input resistance (22), and said input-buffer circuit (24) and internal circuitry (25), The latch signal generating circuit (27) for supplying a latch signal (26) to said latch circuit (25) is provided, and said latch signal generating circuit (27) is characterized by generating a latch signal (26) at the period which an output buffer switches.
[0011]
[Function] Even if a noise is outputted to the period which an output-buffer circuit switches by the resistance of the input resistance (22) connected to an input terminal (21) becoming small from an input-buffer circuit (24) according to the above-mentioned means Since the latch signal (26) generated by the latch signal generating circuit (27) is supplied to the latch circuit (25), a latch circuit (25) will intercept this noise and will carry out latch maintenance of the input signal before noise generating. Therefore, the noise outputted from an input-buffer circuit (24) becomes possible [it not being transmitted to an internal circuitry but preventing malfunction].
[0012]
[Example] Next, the example of this invention is explained with reference to a drawing. Drawing 1 is the circuit diagram showing the input circuit concerning the example of this invention. In drawing 1 , it is the input resistance by which, as for (21), the end was connected to the input terminal, and (22) was

connected to the input terminal (21), and resistance is formed in about R= 300ohms using the refractory metal silicide of low resistance (sheet resistance of about 3ohms) etc. (23) is the N-channel MOS transistor, the drain is connected to other ends of input resistance (22), and both the source and a drain are connected to the touch-down electrical potential difference Vss. (24) is an input-buffer circuit and the input is connected to other ends of input resistance (22). And (25) is a latch circuit and the output of a latch circuit (25) is connected to the internal circuitry to which a latch circuit (25) considers the output of an input-buffer circuit (24) as an input, and does not illustrate it. Moreover, (26) is a latch signal for a data latch supplied to a latch circuit (25). A latch circuit (25) will carry out latch maintenance of the input signal currently outputted from the input-buffer circuit (24), if the input signal outputted from an input-buffer circuit (24) is transmitted to an internal circuitry as it is and a latch signal (26) is outputted, when the latch signal (26) is not outputted. This latch signal (26) is outputted from a latch signal generating circuit (27), and a latch signal generating circuit (27) generates a latch signal (26) at the period which the output-buffer circuit has switched. Thus, the input circuit of this invention is constituted.

[0013] Since according to this configuration the latch signal (26) generated by the latch signal generating circuit (27) is supplied to the latch circuit (25) even if a noise is outputted to the period which the output-buffer circuit has switched when the input resistance (22) connected to the input terminal (21) becomes small from an input-buffer circuit (24), a latch circuit (25) intercepts this noise and carries out latch maintenance of the input signal before noise generating. Therefore, the noise outputted from an input-buffer circuit (24) is not transmitted to an internal circuitry, but can prevent malfunction.

[0014] Drawing 2 is the block diagram showing the example which applied the input circuit constituted as mentioned above to the input circuit of the address terminal of for example, a SRAM (Static Randam Access Memory) semiconductor integrated circuit. In drawing 2 , (21) is an input terminal and becomes the n-bit address input terminal shown by A1-An. (28) is an input circuit concerning this invention shown in drawing 1 , and is applied to the input circuit of the n-bit address input terminal shown by A1-An. Moreover, in this example of application, the latch signal generating circuit (27) shown in drawing 1 corresponded to the delay circuit (29), this delay circuit (29) inputted the ATD signal (37) mentioned later, and the latch signal (26) is generated by delaying an ATD signal (37).

[0015] And an address decoder and (31) are readings of MEMORIDE-TA of the predetermined address with which a ******** decision of a memory matrix and (32) is made at the input signal which is a bus line and was impressed to the address input terminals A1-An, and (30) becomes a line. (33) is an output control circuit, (34) is an output-buffer circuit, and MEMORIDE-TA by which reading appearance was carried out is outputted to an output terminal (35) from this output-buffer circuit (34).

[0016] And it is what (36) is an ATD (Address Transition Detector) circuit and detects change of the input signal inputted into the address input terminals A1-An. This ATD circuit (36) outputs the ATD signal (37) which will serve as a pulse of fixed period high level if change of the input signal inputted into the address input terminals A1-An is detected. This ATD signal (37) is inputted into an output control circuit (33), and equalizes a bus line (32). By the delay circuit (29) mentioned above here considering an ATD signal (37) as an input, and delaying this ATD signal (37), the latch signal (26) doubled with the timing of switching of an output-buffer circuit (34) is generated, and this latch signal (26) is inputted into the latch circuit (25) which constitutes the input circuit section of the n-bit address input terminal shown by A1-An. A delay circuit (29) is made for adjustment of the generating timing of the latch signal (26) which column connection of the inverter of even level is made, and it is constituted, and was doubled with switching of an output-buffer circuit (34) in this example here with the number of stages of the inverter by which column connection is made.

[0017] Drawing 3 is reading of the SRAM semiconductor integrated circuit constituted in this way, and is a wave form chart of operation at the time. With reference to drawing 1 thru/or drawing 3 , the actuation is explained paying attention to the input circuit of this invention. Change of the input signal now impressed to the address input terminals A1-An transmits this input signal to an input-buffer circuit (24). At this time, since the latch signal (26) of a latch circuit (25) is not outputted, a latch circuit (25) transmits an input signal to the address decoder (30) which is an internal circuitry as it is. On the other

hand, an ATD circuit (36) detects that the input signal of the address input terminals A1-An changed, outputs the pulse ATD signal (37) which becomes high-level between 1 commuter's tickets, and this ATD signal (37) is inputted into an output control circuit (33), and it equalizes a bus line (32) on medium level. If an ATD signal (37) is set to a low level after that, equalizing of a bus line (32) will be canceled, reading appearance of MEMORIDE-TA located in the predetermined address based on the input signal impressed to the address input terminals A1-An will be carried out to a bus line (32) from a memory matrix (31), and this data will be outputted from an output-buffer circuit (34). At this time, a power-source noise occurs by switching of an output-buffer circuit (34). Thereby, a noise is outputted from an input-buffer circuit (24). If it is in the conventional input circuit, by transmitting this noise to an internal circuitry, it will be regarded as that from which the address changed, and an ATD circuit (36) outputs an ATD signal (37) again. For this reason, malfunction was caused, when medium level will equalize MEMORIDE-TA by which reading appearance was carried out to the bus line (32) from the memory matrix (31) and the output of an output-buffer circuit (34) became indefinite.

[0018] If it depends on the input circuit of this invention, however, during the period when an output-buffer circuit (34) switches at and the noise is outputted from the input-buffer circuit (24) Since the latch signal (26) which the ATD signal (37) was delayed in the delay circuit (29), and was generated is supplied to the latch circuit (25) A latch circuit (25) becomes the thing which carry out latch maintenance of the input signal before noise generating and to do while intercepting the noise outputted from an input-buffer circuit (24). Even if a noise is outputted to an input-buffer circuit (24) by this, it enables it not to transmit this noise to an internal circuitry, but to prevent malfunction.

[0019]

[Effect of the Invention] By having prepared the latch signal generating circuit (27) for supplying a latch signal (26) to a latch circuit (25) and a latch circuit (25) in the conventional input circuit, when depending on the input circuit of this invention, as explained above Even if the resistance of the input resistance (22) which constitutes an input circuit becomes small and a noise is outputted to an input-buffer circuit (24) by switching of an output-buffer circuit (34) It becomes possible to prevent the transfer to the internal circuitry of this noise, and the semiconductor integrated circuit which prevented malfunction by this can be realized.

[0020] When it furthermore applies to the SRAM semiconductor integrated circuit of the input circuit of this invention, the ATD signal (37) which the SRAM semiconductor integrated circuit originally has can be used for the latch signal (26) supplied to a latch circuit (25), and it can make it only by delaying this ATD signal (37) in a delay circuit (29). For this reason, the special device in a circuit design is not needed, either, but it also has the advantage that the increments in this pattern area are also few, and end.

[Translation done.]

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TECHNICAL FIELD

[Industrial Application] Especially this invention relates to the input circuit which prevented malfunction by the noise generated by switching of an output-buffer circuit in semiconductor integrated circuits, such as SRAM, about a semiconductor integrated circuit.

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PRIOR ART

[Description of the Prior Art] Drawing 4 is drawing showing the general input circuit in semiconductor integrated circuits, such as the conventional SRAM (Static Randam Access Memory). (1) is connected to the internal circuitry to which input resistance and (3) are input-buffer circuits, and an input terminal and (2) do not illustrate the output in drawing. (4) is the N-channel MOS transistor, the drain is connected between the end of input resistance (2), and the input of an input-buffer circuit (3), and both the source and the gate are connected to the touch-down electrical potential difference Vss.
[0003] If it was in the input circuit based on the configuration mentioned above, the main role of input resistance (2) and the N-channel MOS transistor (4) prevents destruction of an input-buffer circuit (3) and the internal circuitry which is not illustrated from the excessive abnormal voltage impressed to an input terminal (1), and, as for the resistance, it was conventionally common as input resistance (2) to have formed in about R=1.5kohm-2.0kohm.
[0004] Moreover, the capacity C1 and C2 shown in drawing 4 is parasitic capacitance formed in a node (a). It is what consists of the wiring capacity of a node (a), the drain diffused-junction capacity of the N-channel MOS transistor (4), the gate capacitance of an input-buffer circuit (3), etc. Capacity C1 exists as supply voltage Vdd and a coupling capacity between nodes (a), and capacity C2 exists as the touch-down electrical potential difference Vss and a coupling capacity between nodes (a).
[0005] By the way, if it is in semiconductor integrated circuits, such as SRAM, in recent years, instead of the conventional poly silicon gate, the gate and wiring are formed by the refractory metal silicide of low resistance etc. for the purpose of improvement in working speed. For this reason, the resistance of input resistance (2) is small as compared with the former. This is because pattern area of input resistance (2) cannot be enlarged in order to raise the accumulation consistency of a semiconductor integrated circuit. However, when the resistance of input resistance (2) became small, the problem of becoming easy to malfunction by the power-source noise by switching of the output-buffer circuit which semiconductor integrated circuits, such as SRAM, have occurred.
[0006] Then, the invention-in-this-application person considered the cause as follows. When an output-buffer circuit switches, a big current flows temporarily in a semiconductor integrated circuit, and this power-source noise happens, when a drop or the touch-down electrical potential difference Vss rises [supply voltage Vdd] by this. For this reason, threshold voltage Vt* of an input-buffer circuit (3) Potential is changed. Since the force of holding the potential of the input signal impressed to the input terminal (1) by the node (a) was comparatively weak when the resistance of input resistance (2) was conventionally formed in R=1.5kohm-2.0kohm and a big value, the potential of threshold voltage Vt* of an input-buffer circuit (3) descends by the drop of supply voltage Vdd, and the potential of a node (a) also descends according to the coupling effectiveness of parasitic capacitance C1.
[0007] On the other hand, the potential of threshold voltage Vt* of an input-buffer circuit (3) rises by lifting of the touch-down electrical potential difference Vss, and the potential of a node (a) also rises according to the coupling effectiveness of parasitic capacitance C2. Therefore, since the potential of the input signal in a node (a) is interlocked with fluctuation of the potential of threshold voltage Vt* of an input-buffer circuit (3) and is changed in the same direction, relation with normal potential of an input

signal and potential of threshold voltage Vt* of an input-buffer circuit (3) in a node (a) is maintained. This had become a comparatively strong thing to the power-source noise by switching of an output-buffer circuit.

[0008] However, if the resistance of input resistance (2) becomes small, the force of holding the potential of the input signal impressed to the input terminal (1) by the node (a) will become strong. The drop of the potential of threshold voltage Vt* of the input-buffer circuit (3) by the drop of supply voltage Vdd, Or it is maintained at potential almost equal to the potential of the input signal which lifting of the potential of threshold voltage Vt* of the input-buffer circuit (3) by lifting of the touch-down electrical potential difference Vss was interlocked with, and the potential of a node (a) stopped being able to change easily in the same direction, and was impressed to the input terminal (1). It becomes impossible for this reason, to maintain the normal relation of the potential of the input signal in a node (a), and the potential of threshold voltage Vt* of an input-buffer circuit (3). For this reason, a noise will be outputted from an input-buffer circuit (3). Drawing 5 is a wave form chart showing generating of this noise of operation. As for (11), in drawing, (12) is the output of an output-buffer circuit about the output of an input-buffer circuit (3) in the input signal with which (10) is impressed to an input terminal (1). For the reason mentioned above when it switched, as the output signal of an output-buffer circuit showed by (13) of drawing 5 now, as shown in (14), a noise will be outputted from an input-buffer circuit (3), and it will be transmitted to an internal circuitry, and becomes the cause of malfunction.

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EFFECT OF THE INVENTION

[Effect of the Invention] By having prepared the latch signal generating circuit (27) for supplying a latch signal (26) to a latch circuit (25) and a latch circuit (25) in the conventional input circuit, when depending on the input circuit of this invention, as explained above Even if the resistance of the input resistance (22) which constitutes an input circuit becomes small and a noise is outputted to an input-buffer circuit (24) by switching of an output-buffer circuit (34) It becomes possible to prevent the transfer to the internal circuitry of this noise, and the semiconductor integrated circuit which prevented malfunction by this can be realized.
[0020] When it furthermore applies to the SRAM semiconductor integrated circuit of the input circuit of this invention, the ATD signal (37) which the SRAM semiconductor integrated circuit originally has can be used for the latch signal (26) supplied to a latch circuit (25), and it can make it only by delaying this ATD signal (37) in a delay circuit (29). For this reason, the special device in a circuit design is not needed, either, but it also has the advantage that the increments in this pattern area are also few, and end.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Thus, if it was in the conventional input circuit, when the resistance of the input resistance (2) which constitutes an input circuit by using the refractory metal silicide of low resistance etc. instead of the conventional polish recon for the purpose of improvement in working speed became small, it had the trouble of becoming easy to produce malfunction, by transmitting the noise outputted by switching of an output-buffer circuit from an input-buffer circuit (3) to an internal circuitry.

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MEANS

[Means for Solving the Problem] The input resistance which it succeeded in this invention in view of the above-mentioned trouble, and was connected to the input terminal (21) (22), The latch circuit connected between the input-buffer circuit (24) connected to said input resistance (22), and said input-buffer circuit (24) and internal circuitry (25), The latch signal generating circuit (27) for supplying a latch signal (26) to said latch circuit (25) is provided, and said latch signal generating circuit (27) is characterized by generating a latch signal (26) at the period which an output buffer switches.

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OPERATION

[Function] Even if a noise is outputted to the period which an output-buffer circuit switches by the resistance of the input resistance (22) connected to an input terminal (21) becoming small from an input-buffer circuit (24) according to the above-mentioned means Since the latch signal (26) generated by the latch signal generating circuit (27) is supplied to the latch circuit (25), a latch circuit (25) will intercept this noise and will carry out latch maintenance of the input signal before noise generating. Therefore, the noise outputted from an input-buffer circuit (24) becomes possible [it not being transmitted to an internal circuitry but preventing malfunction].

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EXAMPLE

[Example] Next, the example of this invention is explained with reference to a drawing. Drawing 1 is the circuit diagram showing the input circuit concerning the example of this invention. In drawing 1 , it is the input resistance by which, as for (21), the end was connected to the input terminal, and (22) was connected to the input terminal (21), and resistance is formed in about R= 300ohms using the refractory metal silicide of low resistance (sheet resistance of about 3ohms) etc. (23) is the N-channel MOS transistor, the drain is connected to other ends of input resistance (22), and both the source and a drain are connected to the touch-down electrical potential difference Vss. (24) is an input-buffer circuit and the input is connected to other ends of input resistance (22). And (25) is a latch circuit and the output of a latch circuit (25) is connected to the internal circuitry to which a latch circuit (25) considers the output of an input-buffer circuit (24) as an input, and does not illustrate it. Moreover, (26) is a latch signal for a data latch supplied to a latch circuit (25). A latch circuit (25) will carry out latch maintenance of the input signal currently outputted from the input-buffer circuit (24), if the input signal outputted from an input-buffer circuit (24) is transmitted to an internal circuitry as it is and a latch signal (26) is outputted, when the latch signal (26) is not outputted. This latch signal (26) is outputted from a latch signal generating circuit (27), and a latch signal generating circuit (27) generates a latch signal (26) at the period which the output-buffer circuit has switched. Thus, the input circuit of this invention is constituted.
[0013] Since according to this configuration the latch signal (26) generated by the latch signal generating circuit (27) is supplied to the latch circuit (25) even if a noise is outputted to the period which the output-buffer circuit has switched when the input resistance (22) connected to the input terminal (21) becomes small from an input-buffer circuit (24), a latch circuit (25) intercepts this noise and carries out latch maintenance of the input signal before noise generating. Therefore, the noise outputted from an input-buffer circuit (24) is not transmitted to an internal circuitry, but can prevent malfunction.
[0014] Drawing 2 is the block diagram showing the example which applied the input circuit constituted as mentioned above to the input circuit of the address terminal of for example, a SRAM (Static Randam Access Memory) semiconductor integrated circuit. In drawing 2 , (21) is an input terminal and becomes the n-bit address input terminal shown by A1-An. (28) is an input circuit concerning this invention shown in drawing 1 , and is applied to the input circuit of the n-bit address input terminal shown by A1-An. Moreover, in this example of application, the latch signal generating circuit (27) shown in drawing 1 corresponded to the delay circuit (29), this delay circuit (29) inputted the ATD signal (37) mentioned later, and the latch signal (26) is generated by delaying an ATD signal (37).
[0015] And an address decoder and (31) are readings of MEMORIDE-TA of the predetermined address with which a ******** decision of a memory matrix and (32) is made at the input signal which is a bus line and was impressed to the address input terminals A1-An, and (30) becomes a line. (33) is an output control circuit, (34) is an output-buffer circuit, and MEMORIDE-TA by which reading appearance was carried out is outputted to an output terminal (35) from this output-buffer circuit (34).
[0016] And it is what (36) is an ATD (Address Transition Detector) circuit and detects change of the input signal inputted into the address input terminals A1-An. This ATD circuit (36) outputs the ATD

signal (37) which will serve as a pulse of fixed period high level if change of the input signal inputted into the address input terminals A1-An is detected. This ATD signal (37) is inputted into an output control circuit (33), and equalizes a bus line (32). By the delay circuit (29) mentioned above here considering an ATD signal (37) as an input, and delaying this ATD signal (37), the latch signal (26) doubled with the timing of switching of an output-buffer circuit (34) is generated, and this latch signal (26) is inputted into the latch circuit (25) which constitutes the input circuit section of the n-bit address input terminal shown by A1-An. A delay circuit (29) is made for adjustment of the generating timing of the latch signal (26) which column connection of the inverter of even level is made, and it is constituted, and was doubled with switching of an output-buffer circuit (34) in this example here with the number of stages of the inverter by which column connection is made.

[0017] Drawing 3 is reading of the SRAM semiconductor integrated circuit constituted in this way, and is a wave form chart of operation at the time. With reference to drawing 1 thru/or drawing 3 , the actuation is explained paying attention to the input circuit of this invention. Change of the input signal now impressed to the address input terminals A1-An transmits this input signal to an input-buffer circuit (24). At this time, since the latch signal (26) of a latch circuit (25) is not outputted, a latch circuit (25) transmits an input signal to the address decoder (30) which is an internal circuitry as it is. On the other hand, an ATD circuit (36) detects that the input signal of the address input terminals A1-An changed, outputs the pulse ATD signal (37) which becomes high-level between 1 commuter's tickets, and this ATD signal (37) is inputted into an output control circuit (33), and it equalizes a bus line (32) on medium level. If an ATD signal (37) is set to a low level after that, equalizing of a bus line (32) will be canceled, reading appearance of MEMORIDE-TA located in the predetermined address based on the input signal impressed to the address input terminals A1-An will be carried out to a bus line (32) from a memory matrix (31), and this data will be outputted from an output-buffer circuit (34). At this time, a power-source noise occurs by switching of an output-buffer circuit (34). Thereby, a noise is outputted from an input-buffer circuit (24). If it is in the conventional input circuit, by transmitting this noise to an internal circuitry, it will be regarded as that from which the address changed, and an ATD circuit (36) outputs an ATD signal (37) again. For this reason, malfunction was caused, when medium level will equalize MEMORIDE-TA by which reading appearance was carried out to the bus line (32) from the memory matrix (31) and the output of an output-buffer circuit (34) became indefinite.

[0018] If it depends on the input circuit of this invention, however, during the period when an output-buffer circuit (34) switches at and the noise is outputted from the input-buffer circuit (24) Since the latch signal (26) which the ATD signal (37) was delayed in the delay circuit (29), and was generated is supplied to the latch circuit (25) A latch circuit (25) becomes the thing which carry out latch maintenance of the input signal before noise generating and to do while intercepting the noise outputted from an input-buffer circuit (24). Even if a noise is outputted to an input-buffer circuit (24) by this, it enables it not to transmit this noise to an internal circuitry, but to prevent malfunction.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
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3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the circuit diagram showing the input circuit concerning the example of this invention.
[Drawing 2] It is the block diagram showing the example of application to the SRAM semiconductor integrated circuit of the input circuit of this invention.
[Drawing 3] It is a wave form chart of operation for explaining the actuation in the example of application to the SRAM semiconductor integrated circuit of the input circuit of this invention.
[Drawing 4] It is the circuit diagram showing the input circuit concerning the conventional example.
[Drawing 5] It is the wave form chart of the input circuit of the conventional example of operation.
[Description of Notations]
21 : Input Terminal
22 : Input Resistance
23 : N-channel MOS Transistor
24 : Input-Buffer Circuit
25 : Latch Circuit
26 : Latch Signal
27 : Latch Signal Generating Circuit
Vss : touch-down electrical potential difference

[Translation done.]

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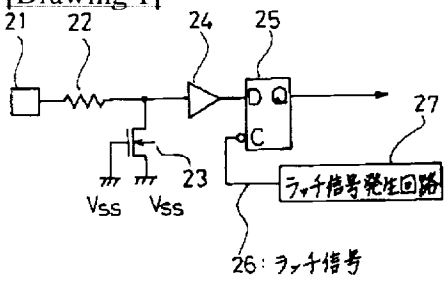
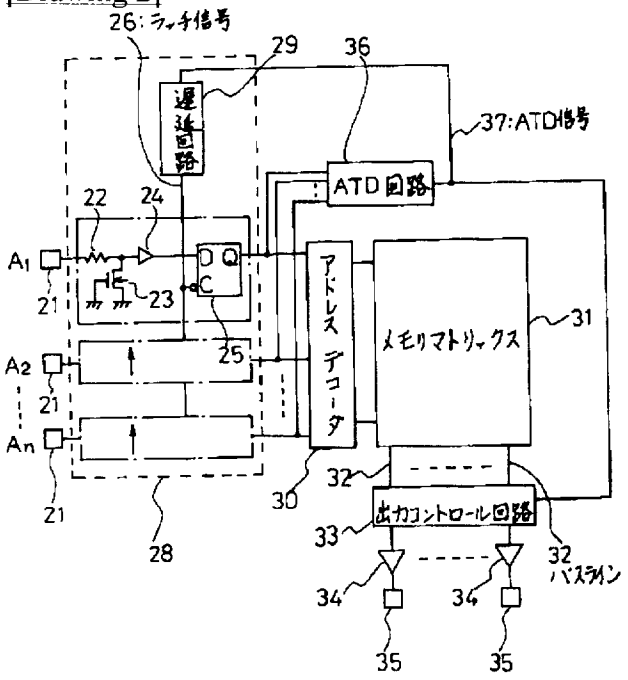
DRAWINGS

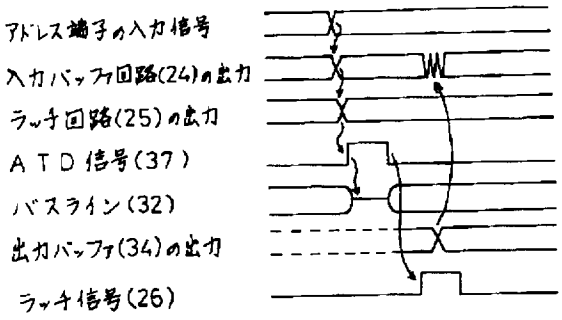
[Drawing 1]



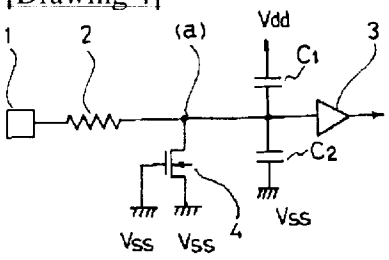
[Drawing 2]



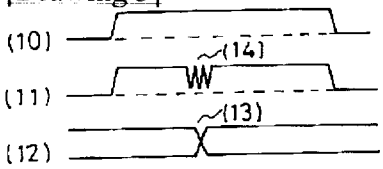
[Drawing 3]



[Drawing 4]



[Drawing 5]



[Translation done.]